

X2 Dual SC Optical Transceivers

Introduction

This design guide provides the information needed to incorporate OptixCom's fiber optics transceiver products in the customer's system. The X2 series of the transceiver products are compliant with the X2 multi-source agreement. For more detail information, please refer to the URL <http://207.158.200.152//SFP/SFP%20MSA.pdf> or visit OptixCom web site: <http://www.OptixCom.com> for the official documentation. As the X2 transceiver is a compact version of the XENPAK, more technical details are also available in the OptixCom's website with XENPAK Design Guide.

The reference guide covers the following topics:

A.Pin Assignment & Description

B.Package Outline

C.Host Board & Electrical Connector Mechanical Layout

D.Optical Interface

E.Mechanical Forces

F.Transceiver and Connector Durability

G.PMD Support

H.X2 Electrical Interface



A. Pin Assignment & Description

The X2 transceiver contains a printed circuit board that mates with the 70-pin electrical connector. The pads are designed for a sequenced mating:

- First mate - ground contacts
- Second mate - power contacts
- Third mate - signal contacts

A. Pin Assignment & Description

Pin No	Name	Dir	Function	Notes
1	GND		Electrical Ground	1
2	GND		Electrical Ground	1
3	GND		Electrical Ground	1
4	5.0V		Power	2
5	3.3V		Power	2
6	3.3V		Power	2
7	APS =1.2V		Adaptive Power Supply	2
8	APS =1.2V		Adaptive Power Supply	2
9	LASI		Open Drain Compatible 10K-22K pull up on host. Logic High: Normal Operation Logic Low: LASI Asserted	4
10	RESET	I	Open Drain compatible. 10-22K pull-up on transceiver Logic high = Normal operation Logic low = Reset Minimum reset assert time 1 ms	4
11	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8
12	TX ON/OFF	I	Open Drain compatible. 10-22K pull-up on transceiver Logic high = Transmitter On (capable) Logic low = Transmitter Off (always)	4
13	RESERVED		Reserved	4
14	MOD DETECT	O	Pulled low inside module through 1k	
15	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8
16	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8
17	MDIO	I/O	Management Data IO	4, 5
18	MDC	I	Management Data Clock	4, 5
19	PRTAD4	I	Port Address Bit 4 (Low = 0)	4
20	PRTAD3	I	Port Address Bit 3 (Low = 0)	4
21	PRTAD2	I	Port Address Bit 2 (Low = 0)	4
22	PRTAD1	I	Port Address Bit 1 (Low = 0)	4
23	PRTAD0	I	Port Address Bit 0 (Low = 0)	4
24	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8
25	APS SET		Feedback input for APS	
26	RESERVED		Reserved for Avalanche Photodiode use.	8
27	APS SENSE		APS Sense Connection	

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28	APS =1.2V		Adaptive Power Supply	2
29	APS =1.2V		Adaptive Power Supply	2
30	3.3V		Power	2
31	3.3V		Power	2
32	5.0V		Power	2
33	GND		Electrical Ground	1
34	GND		Electrical Ground	1
35	GND		Electrical Ground	1
36	GND		Electrical Ground	1
37	GND		Electrical Ground	1
38	RESERVED		Reserved	
39	RESERVED		Reserved	
40	GND		Electrical Ground	1
41	RX LANE0+	O	Module XAUI Output Lane 0+	7
42	RX LANE0-	O	Module XAUI Output Lane 0-	7
43	GND		Electrical Ground	1
44	RX LANE1+	O	Module XAUI Output Lane 1+	7
45	RX LANE1-	O	Module XAUI Output Lane 1-	7
46	GND		Electrical Ground	1
47	RX LANE2+	O	Module XAUI Output Lane 2+	7
48	RX LANE2-	O	Module XAUI Output Lane 2-	7
49	GND		Electrical Ground	1
50	RX LANE3+	O	Module XAUI Output Lane 3+	7
51	RX LANE3-	O	Module XAUI Output Lane 3-	7
52	GND		Electrical Ground	1
53	GND		Electrical Ground	1
54	GND		Electrical Ground	1
55	TX LANE0+	I	Module XAUI Input Lane 0+	7
56	TX LANE0-	I	Module XAUI Input Lane 0-	7
57	GND		Electrical Ground	1
58	TX LANE1+	I	Module XAUI Input Lane 1+	7
59	TX LANE1-	I	Module XAUI Input Lane 1-	7
60	GND		Electrical Ground	1
61	TX LANE2+	I	Module XAUI Input Lane 2+	7
62	TX LANE2-	I	Module XAUI Input Lane 2-	7
63	GND		Electrical Ground	1

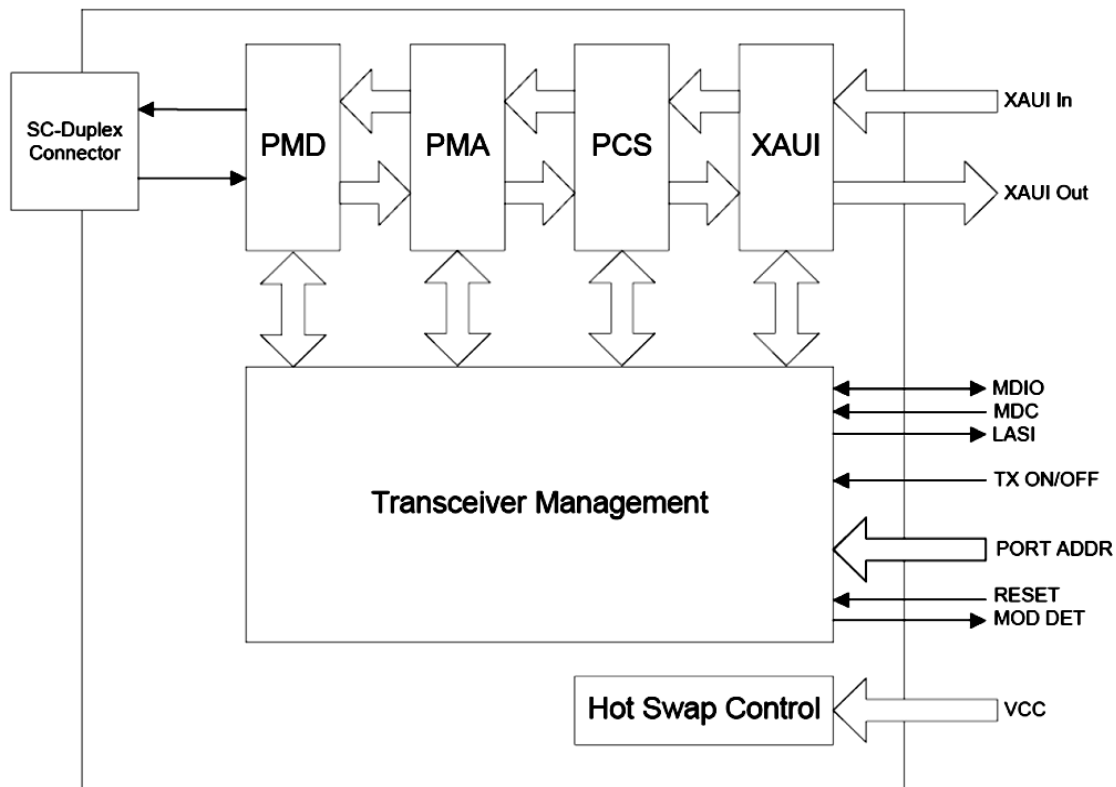
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64	TX LANE3+	I	Module XAUI Input Lane 3+	7
65	TX LANE3-	I	Module XAUI Input Lane 3-	7
66	GND		Electrical Ground	1
67	RESERVED		Reserved	
68	RESERVED		Reserved	
69	GND		Electrical Ground	1
70	GND		Electrical Ground	1

Notes:

- 1) Ground connections are common for TX and RX.
- 2) All connector contacts are rated at 0.5A nominal.
- 3) 1.2V CMOS compatible.
- 4) MDIO and MDC timing must comply with IEEE802.3ae Clause 45.3.
- 5) XAUI output characteristics should comply with IEEE802.3ae Clause 47.
- 6) Transceivers will be MSA compliant when no signals are present on the vendor specific pins.



Functional Diagram

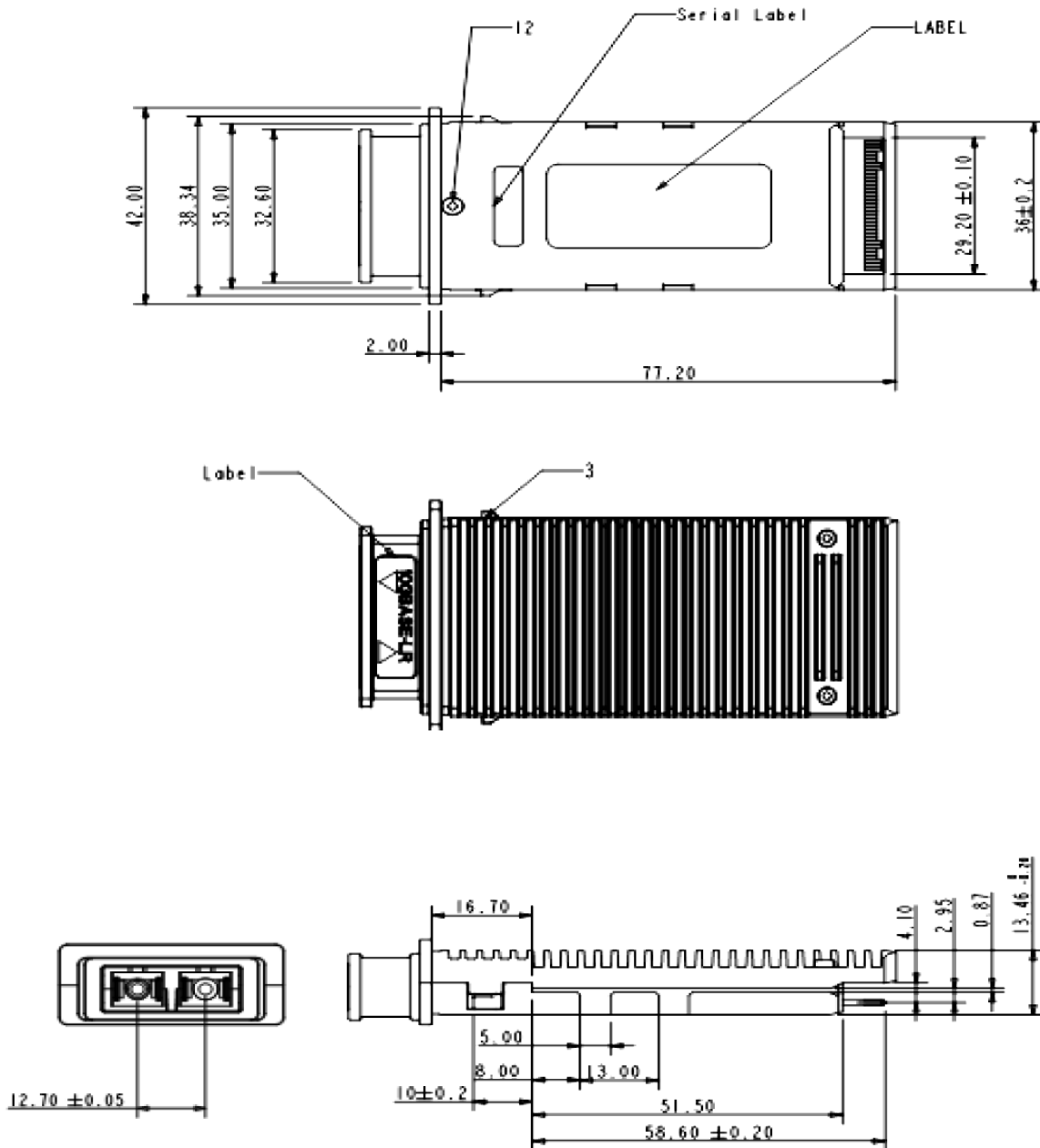
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70	GND	1	GND
69	GND	2	GND
68	RESERVED	3	GND
67	RESERVED	4	5.0V
66	GND	5	3.3V
65	TX LANE3-	6	3.3V
64	TX LANE3+	7	APS
63	GND	8	APS
62	TX LANE2-	9	LASI
61	TX LANE2+	10	RESET
60	GND	11	VEND SPECIFIC
59	TX LANE1-	12	TX ON/OFF
58	TX LANE1+	13	RESERVED
57	GND	14	MOD DETECT
66	TX LANE0	15	VEND SPECIFIC
55	TX LANE0+	16	VEND SPECIFIC
54	GND	17	MDIO
53	GND	18	MDC
52	GND	19	PRTAD4
51	RX LANE3-	20	PRTAD3
50	RX LANE3+	21	PRTAD2
49	GND	22	PRTAD1
48	RX LANE2-	23	PRTAD0
47	RX LANE2+	24	VEND SPECIFIC
46	GND	25	APS SET
45	RX LANE1-	26	RESERVED
44	RX LANE1+	27	APS SENSE
43	GND	28	APS
42	RX LANE0-	29	APS
41	RX LANE0+	30	3.3V
40	GND	31	3.3V
39	RESERVED	32	5.0V
38	RESERVED	33	GND
37	GND	34	GND
36	GND	35	GND

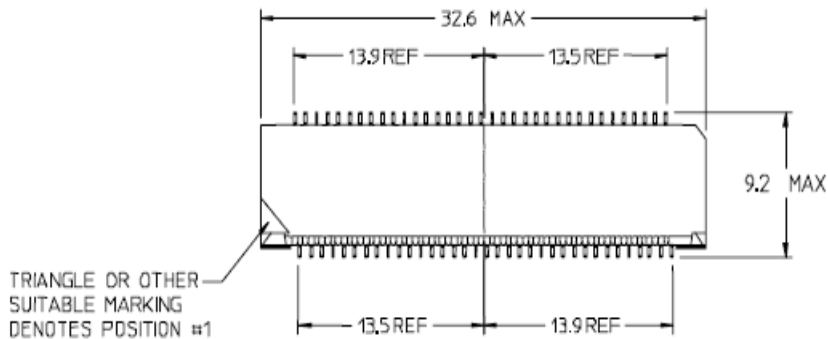
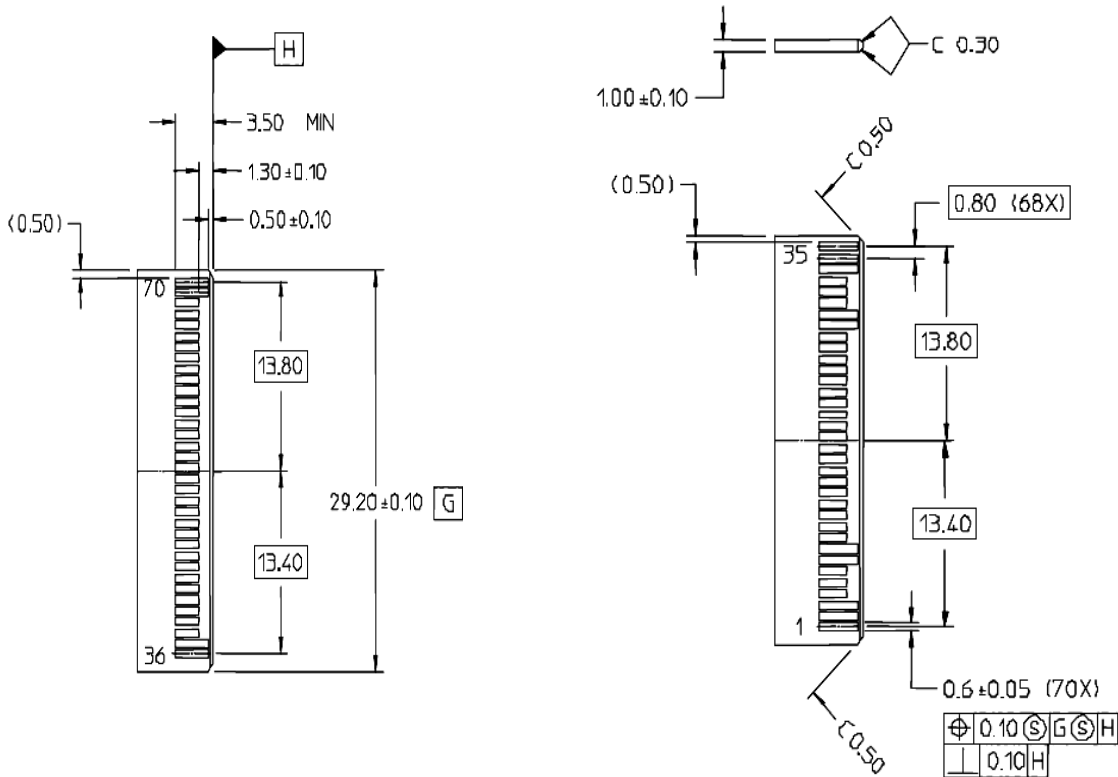
X2 Transceiver Pad Layout

B. Package Outline



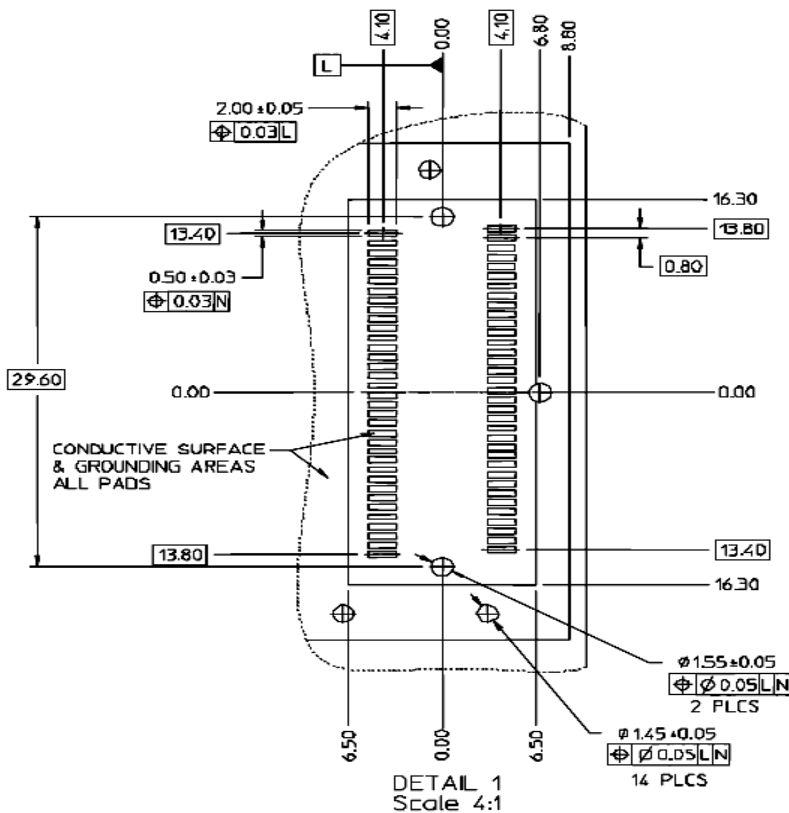
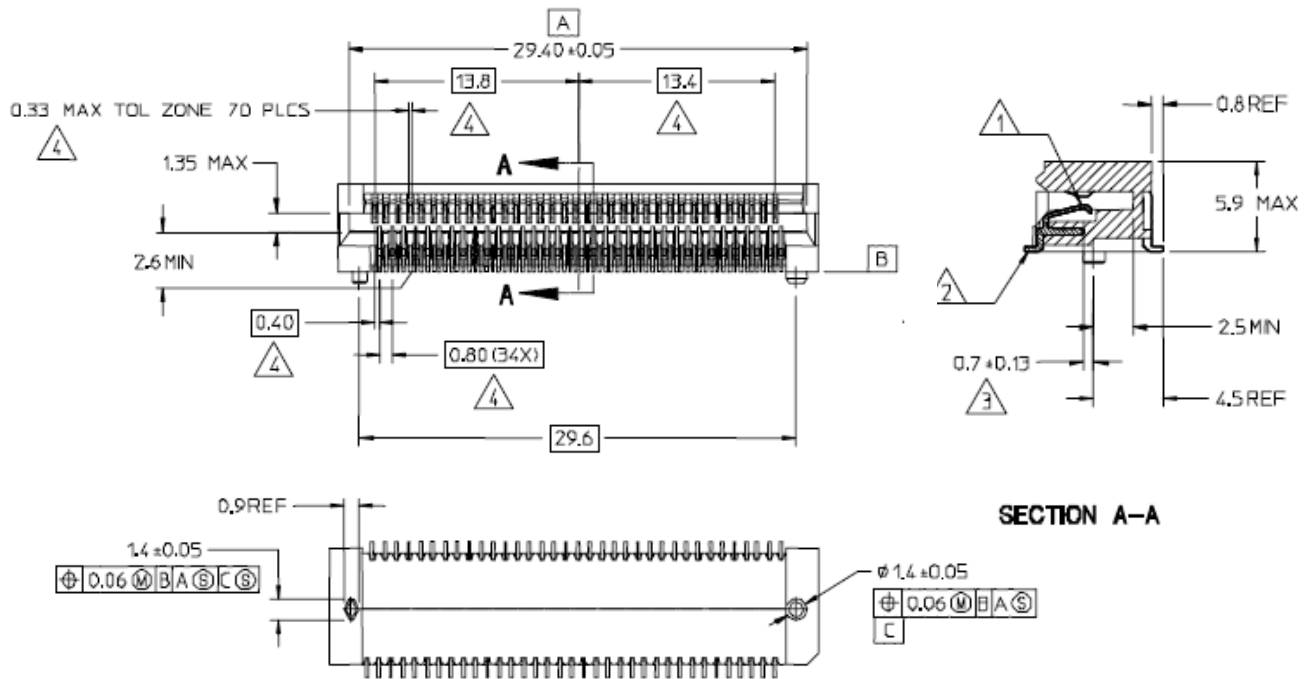
Unit: mm, typical tolerance for these dimensions is ± 0.2 mm

C. Host Board & Electrical Connector Mechanical Layout

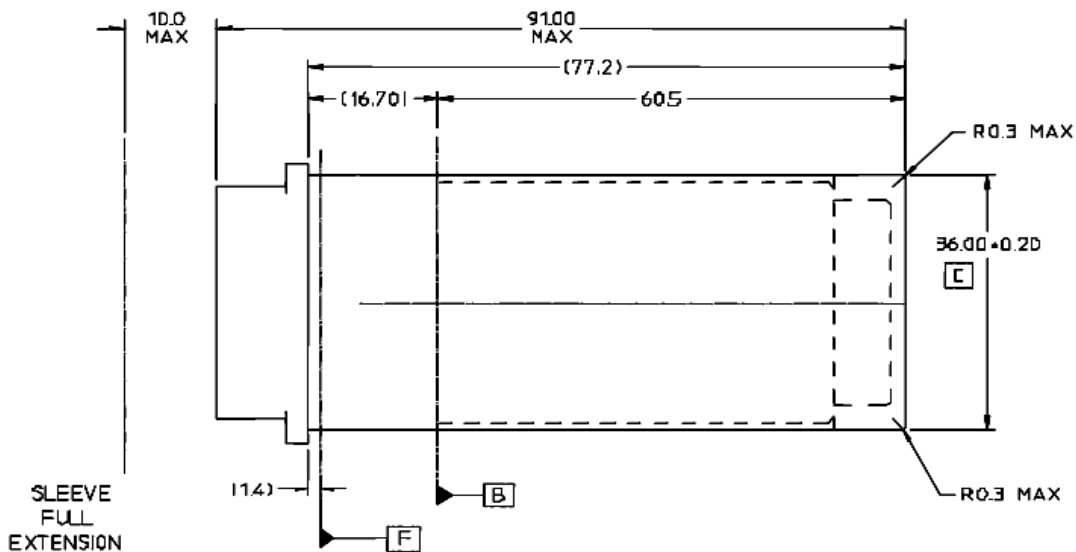
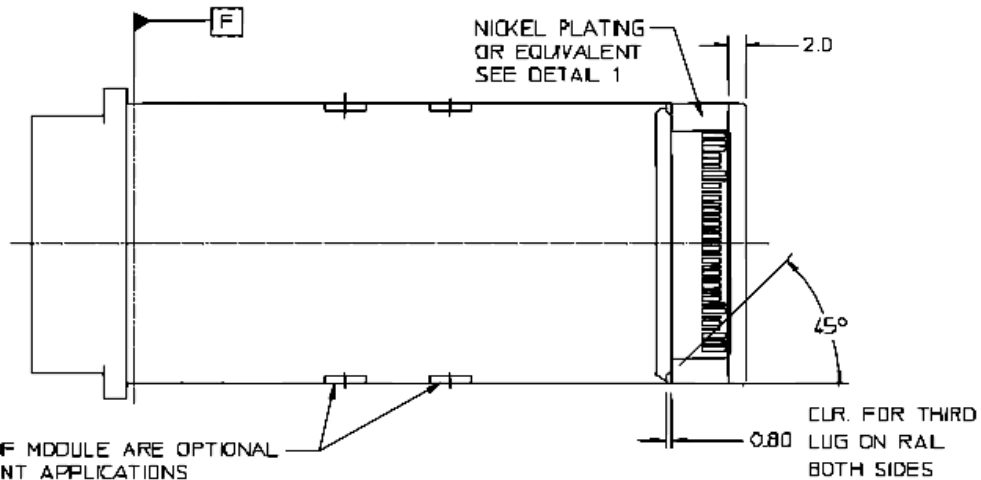
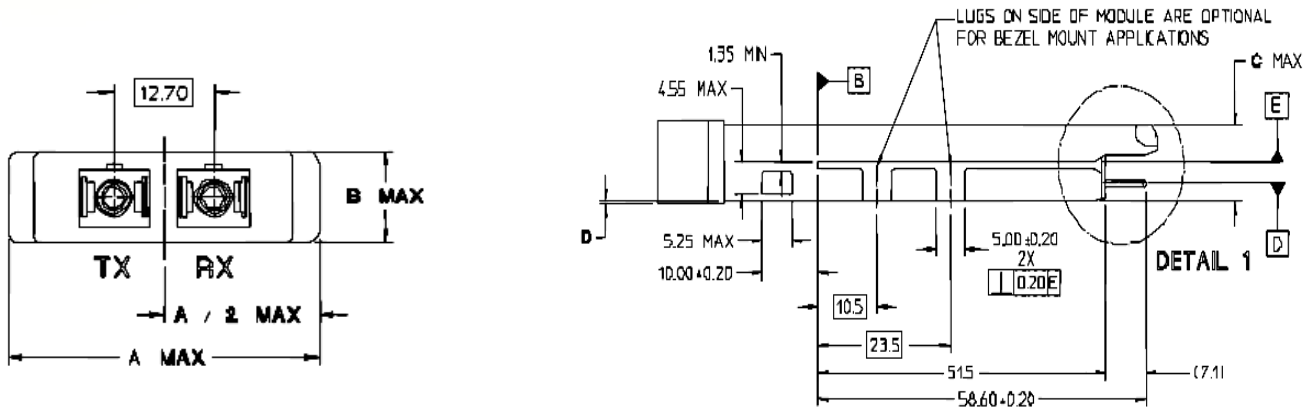


- ① PLATING IN CONTACT AREA:
0.38 MICROMETERS MIN THK OVER
2.54 MICROMETERS MIN THK NICKEL
- ② PLATING ON SOLDER FOOT AREA:
GOLD FLASH OVER 2.54 MICROMETERS
MIN THK NICKEL
- ③ DIMENSION TO POINT OF SPRING
ENGAGEMENT FOR TOP AND BOTTOM ROWS
- ④ CONTACT MUST BE WITHIN 0.33 WIDE
TOLERANCE ZONE. THE CENTERLINE OF
THE TOLERANCE ZONE IS DEFINED BY
THE INDICATED BASIC DIMENSIONS RELATIVE
TO DATUM A REGARDLESS OF FEATURE SIZE.

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D. Optical Interface

The purpose of this section is to specify the optical connector interface sufficiently to insure performance, inter-mateability and supplier flexibility.

Optical Plug

- The Optical Interface shall use a duplex SC optical plug which conforms to IEC 61754-4. Only the floating duplex style connector plug shall be used. Rigid SC duplex connectors shall not be used. Connector keys are used for transmit/receive polarity.
- NOTE: Floating Duplex SC connectors may use two simplex connectors and mechanical coupling to create a single connector that retains both connectors but allows them to "float" within the specified tolerance.

Optical Receptacle

- The Objective of this section is to specify the optical connector interface to sufficiently ensure performance, inter-mateability and maximum supplier flexibility.

Optical Receptacle

- The SC Duplex Receptacle shall conform to the requirements of IEC 61754-4 with the following clarification:
- The distance between the center line of the active optical bores (ref DB) shall be 12.25/13.15mm to match the floating duplex SC optical plug. Increasing this tolerance avoids the restrictive manufacturing tolerance associated with rigid SC connectors.

E. Mechanical Forces

This following limits should be observed when designing for, or using X2 transceivers:

Forces are defined for module inserted in correct intended orientation:

- 1) Maximum insertion force = 80N
- 2) Maximum retention force = 50N
- 3) Maximum retention force with latch engaged = 100N

Force defined for module when inserted incorrectly:

- 1) Force to insert module when upside down must be > 100N

Rail extraction force must be greater than 14.3N per pin.

F. Transceiver and Connector Durability

The following life ratings should be observed when designing for, or using, X2 transceivers and their associated connectors:

Minimum mate/de-mate cycles for transceiver = 50 cycles

Minimum mate/de-mate cycles for 70 pin connector = 100 cycles

G. PMD Support

This MSA aims to accommodate all XAUI based 10GbE applications.

In order to support multiple interface types the MSA defines 3 different power classes, namely:-

- Class I: up-to 4W maximum power dissipation
- Class II: 4-5W maximum power dissipation
- Class III: >5W maximum power dissipation

The appropriate package style (lo, mid or hi) should be selected depending on the power class of the parts used and the thermal environment of the particular design.

It should be noted that the thermal capacity of the X2 is lower than XENPAK.

H. X2 Electrical Interface

The X2 connector is identical to XENPAK, for example TycoAMP Part number 1367337-1, Molex Part No. 74441-0003 or equivalent.

An X2 module will be electrically identical to XENPAK module apart from the following modifications: -

X2 Register Set Relative to XENPAK MSA

The X2 register map is identical to XENPAK.

The contents are equivalent to a XENPAK transceiver except:

- The package OUI, register D.32818 (decimal) D.8032 (hex) is "00-0c-64", (note this is different from the XENPAK OUI which is 00-08-BE).
- X2 transceiver will use a 00000010 (binary), 0x02 (hex) mask in register d.32786 (decimal) D.8012 (hex) to indicate transceiver type (versus XENPAK which uses 0x01 (hex)).